Redundant Via Insertion with Wire Bending

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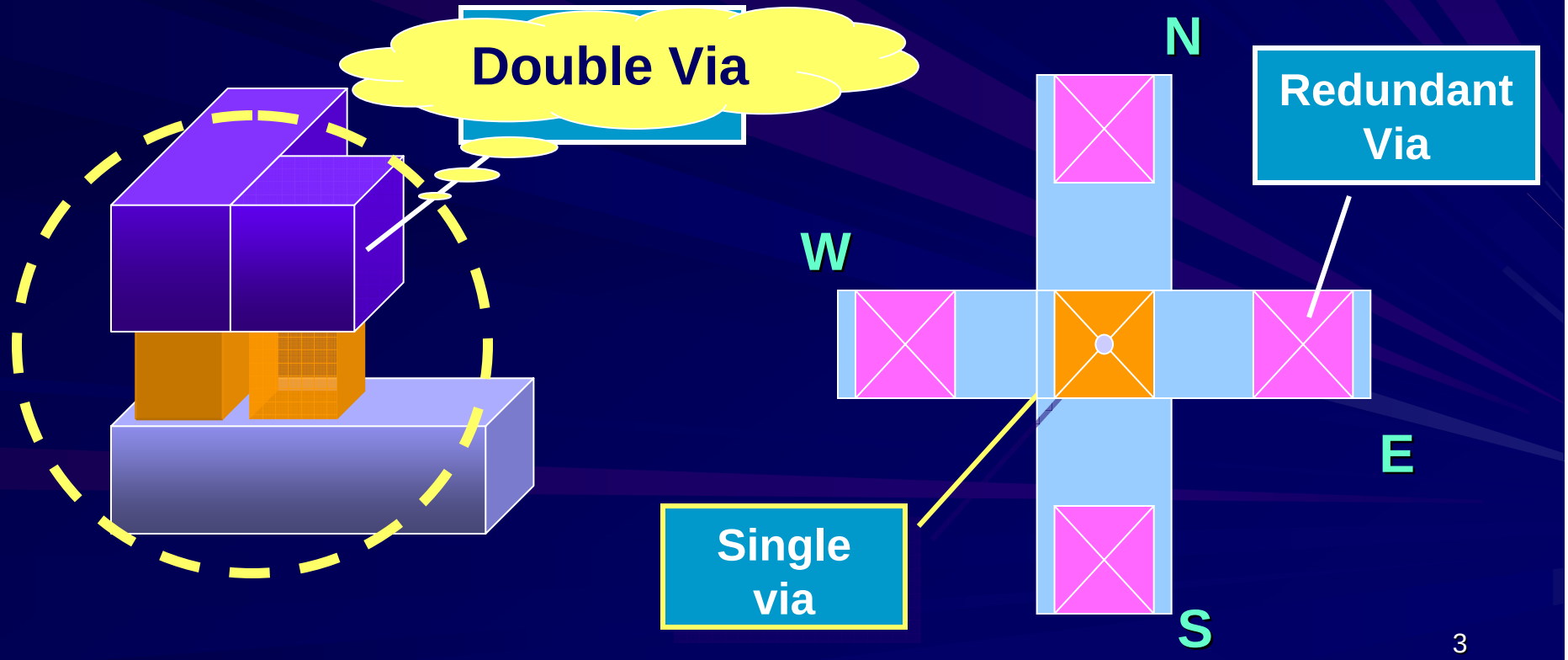
Outline

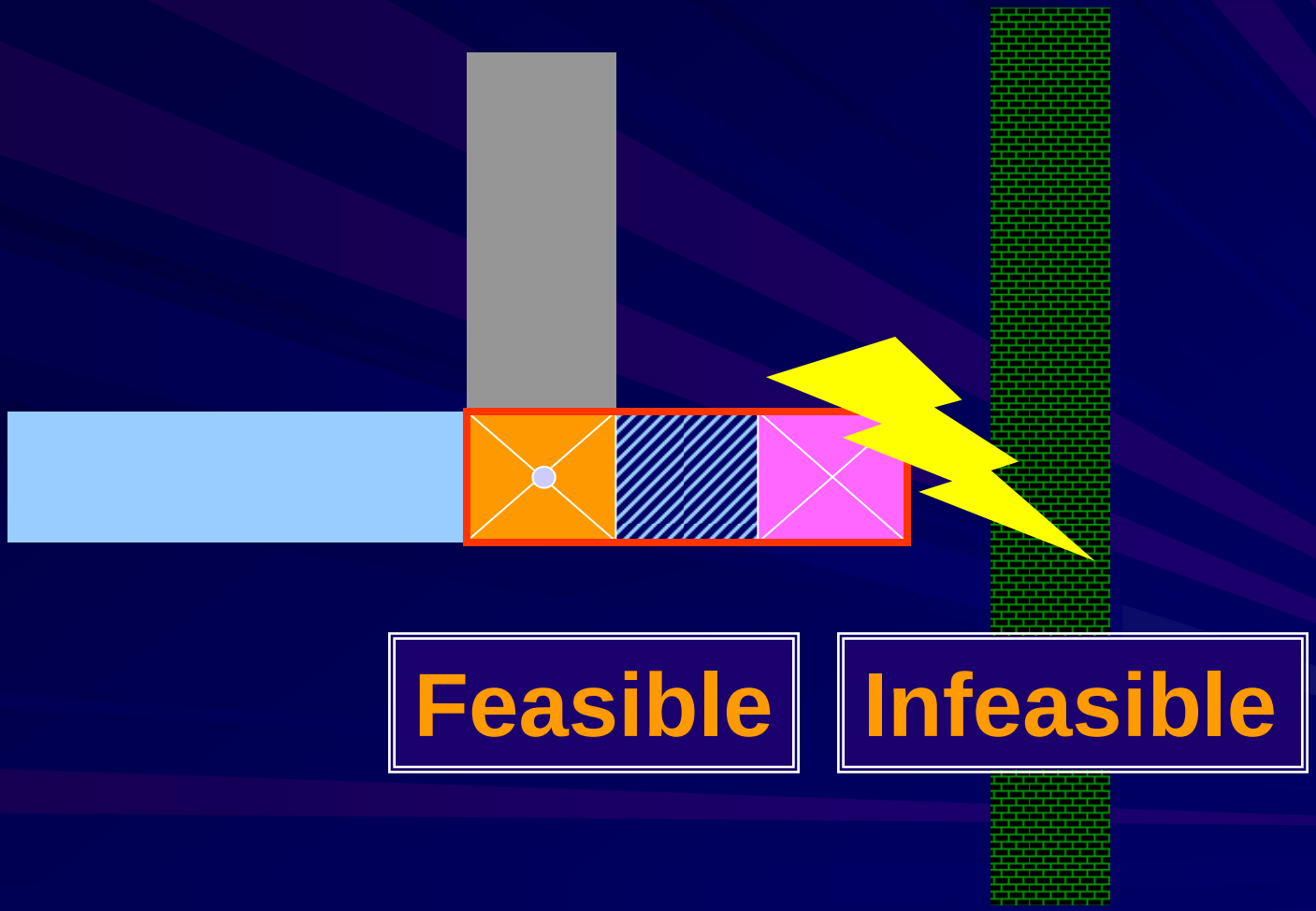
- Preliminaries
- Problem definition
- Minimum-weight maximum independent set formulation
- 0-1 integer linear program based approach
- Experimental results
- Conclusion

Redundant via

- Enable a single via failure to be tolerated
- Improve the chip yield and reliability



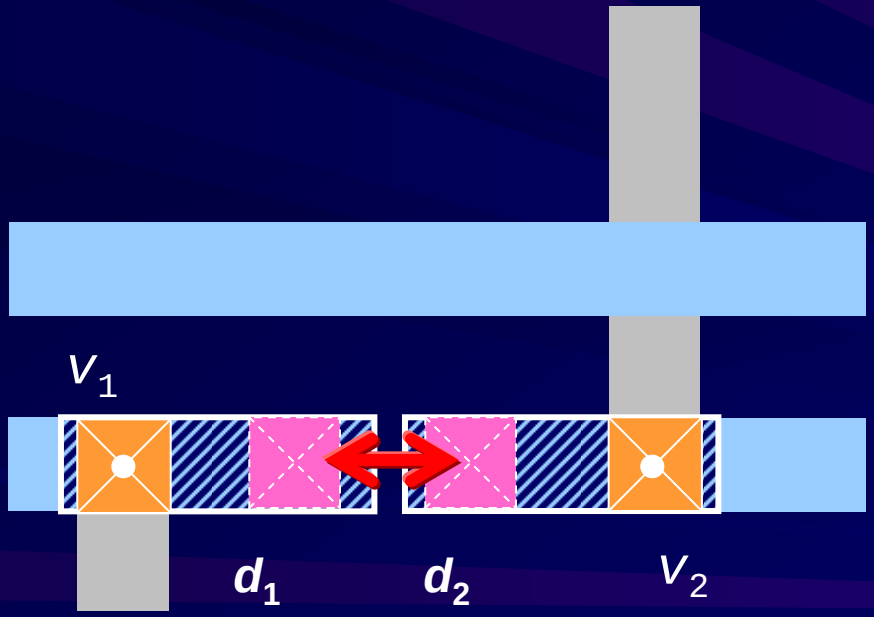
Feasible double via



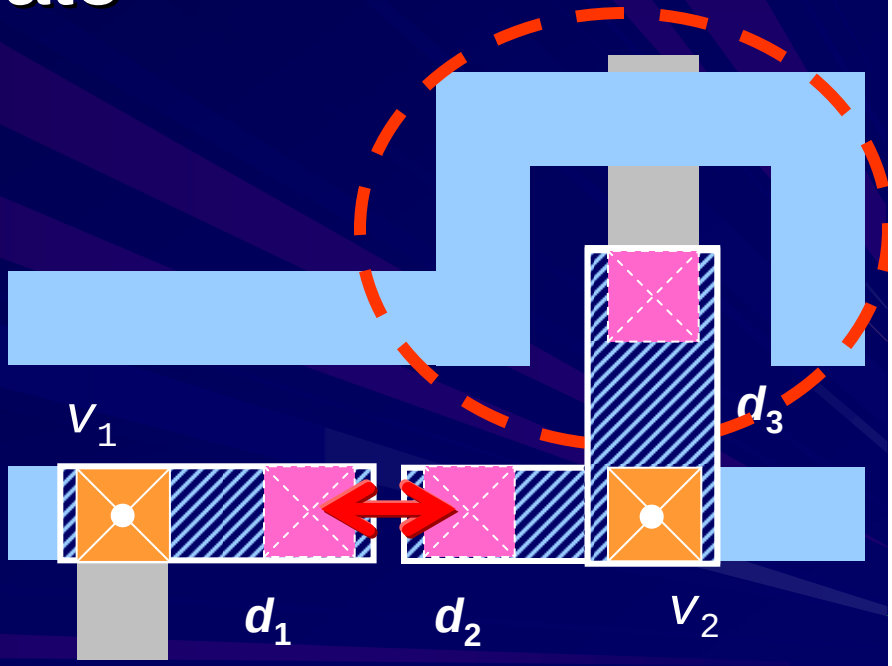
Feasible **Infeasible**

Wire bending

- Create more feasible double vias
- Improve the insertion rate



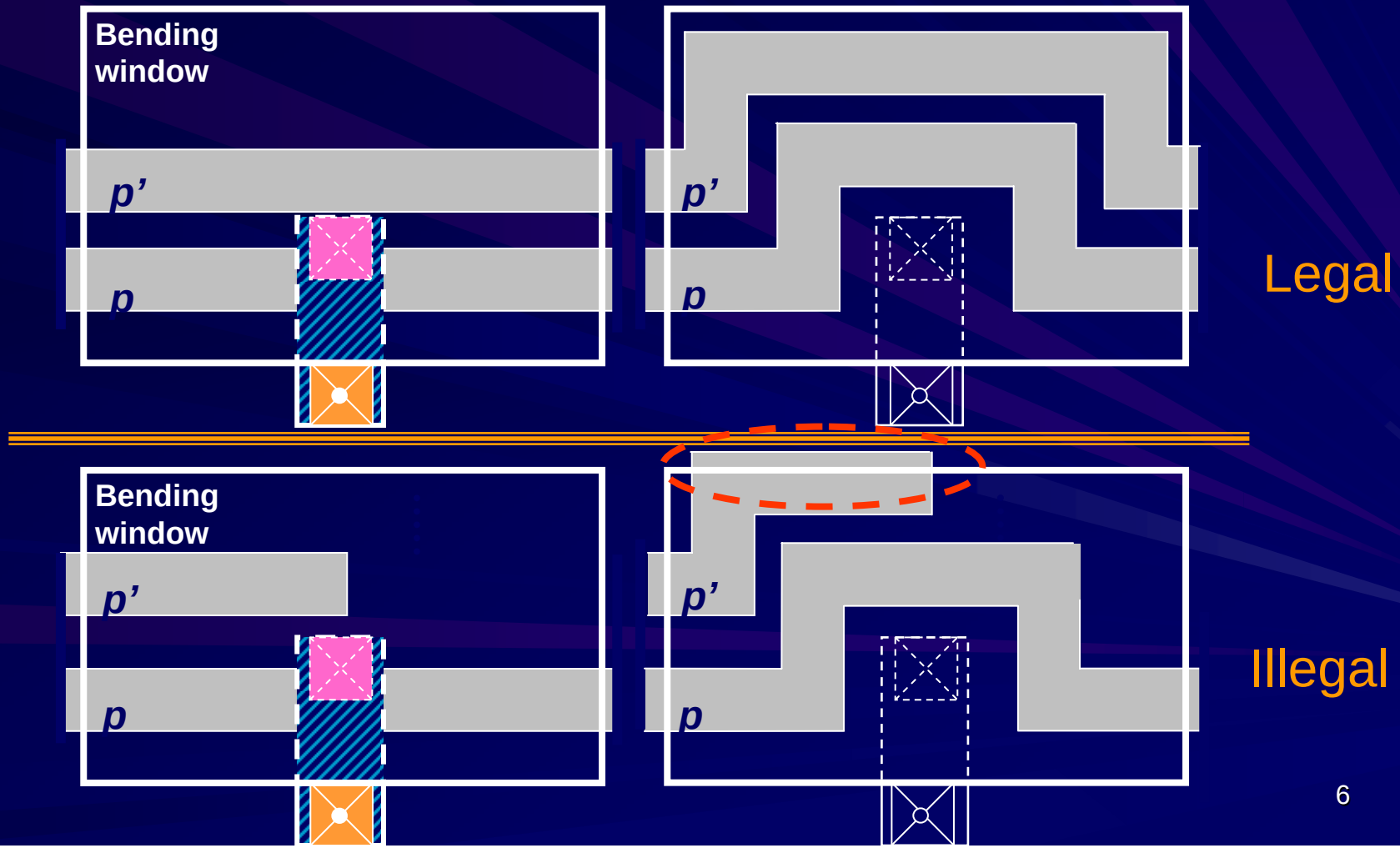
Insertion rate = 50%



Insertion rate = 100%

Wire bending (cont'd)

- The wires are allowed to be bent
- A bending window of pre-defined size is given

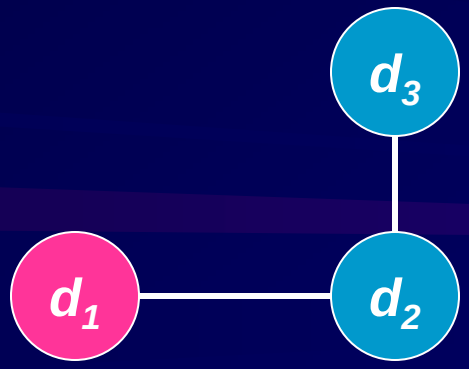


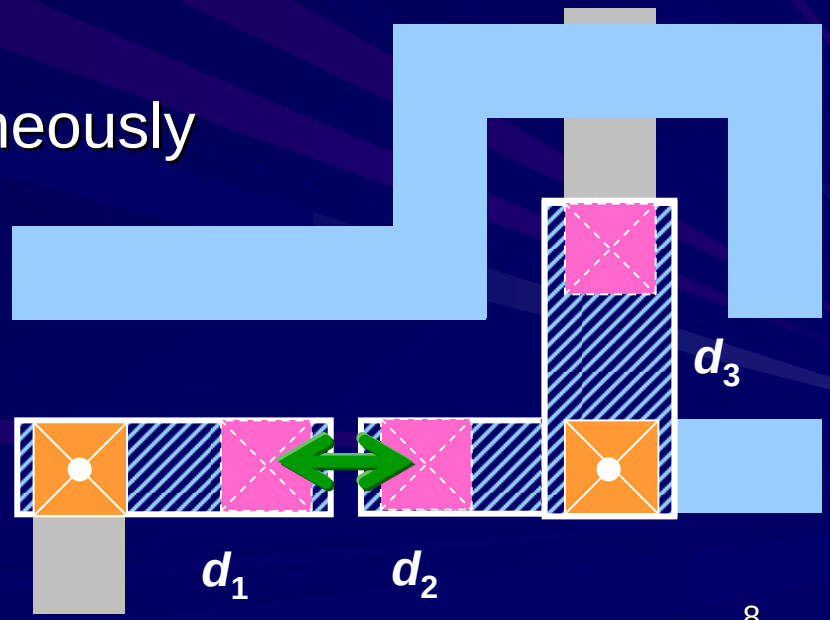
Double via insertion with wire bending (DVI/WB)

- **Input**
  - A routed design and a set of via-related design rules
- **Goal**
  1. To replace as many single vias with double vias as possible
  2. Minimize the wirelength increase due to wire bending
- **Constraints**
  - Each single via either remains unchanged or is replaced by a double via
  - After via replacement and wire bending, no design rule is violated

Enhanced conflict graph

- An undirected vertex-weighted graph constructed from a detailed routing solution
- Vertex
  - a feasible double via
- Edge
  - cannot be inserted simultaneously

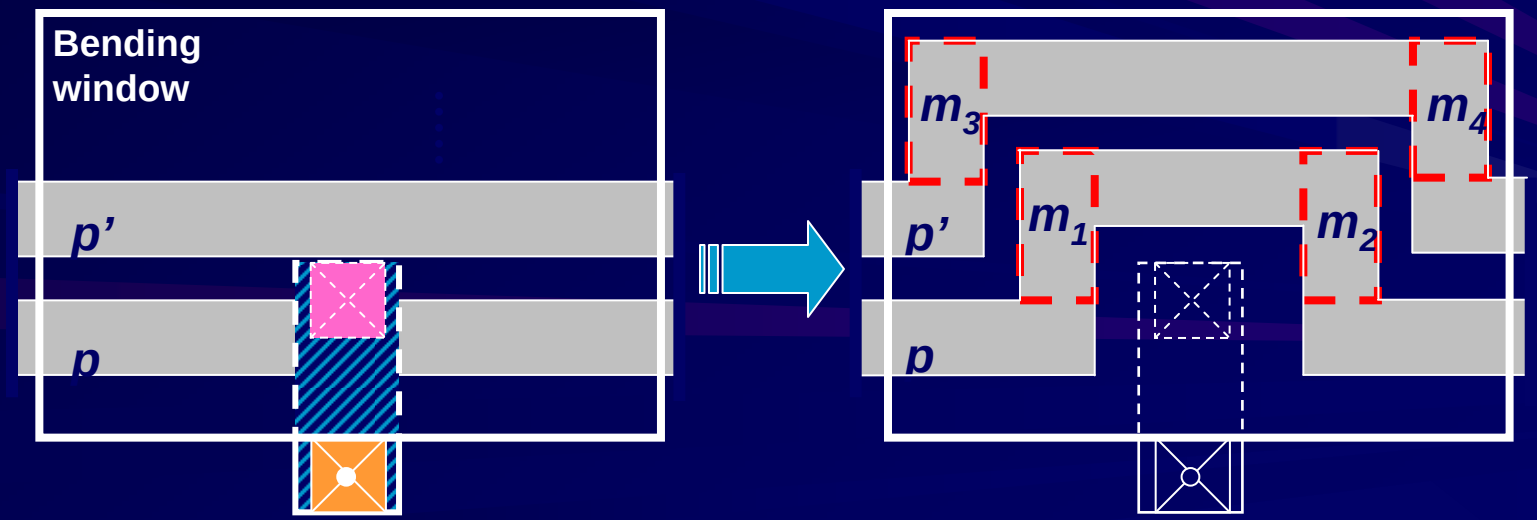




Enhanced conflict graph

- Each vertex is associated with a weight
  - The amount of wirelength increase caused by inserting the corresponding double via

$$Weight = m_1+m_2+m_3+m_4$$

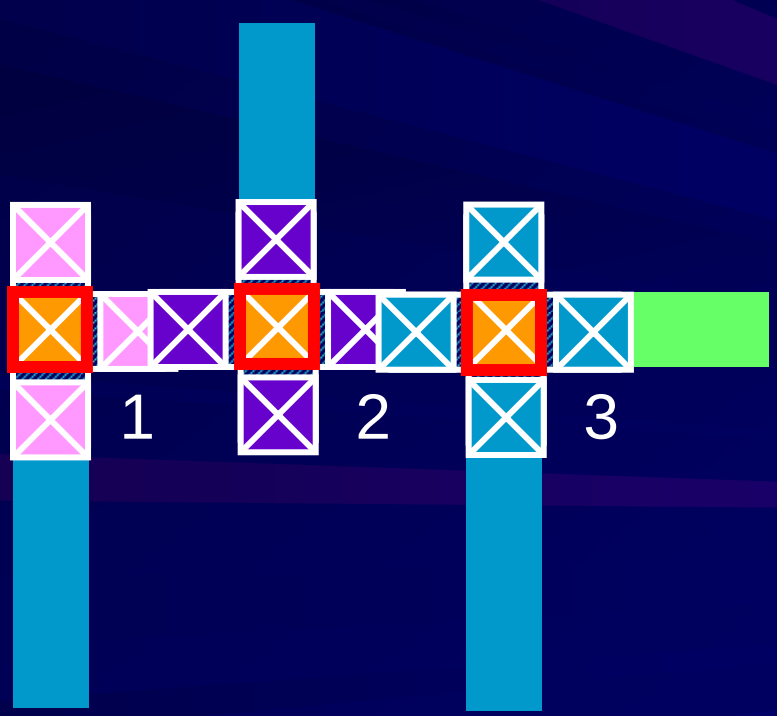


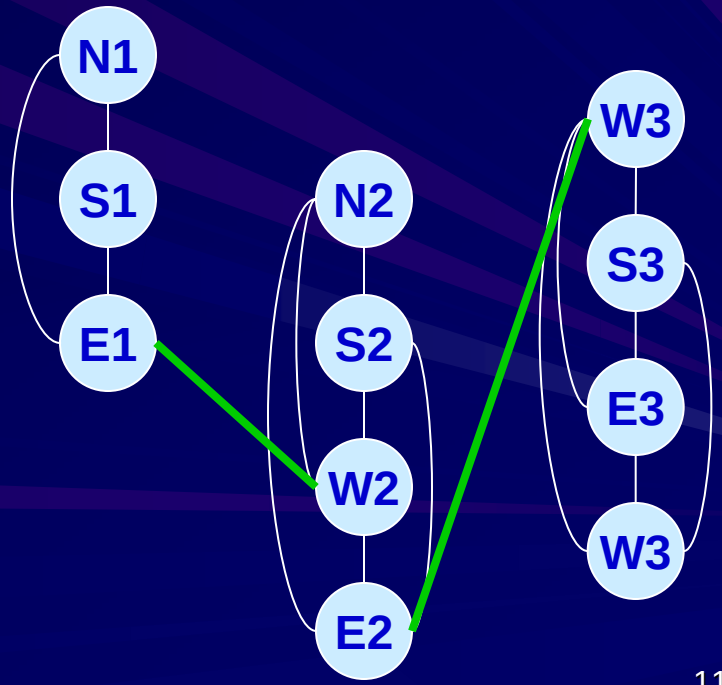
Theorem

- The DVI/WB problem can be formulated as that of finding a minimum-weight maximum independent set (mWMIS) from the enhanced conflict graph

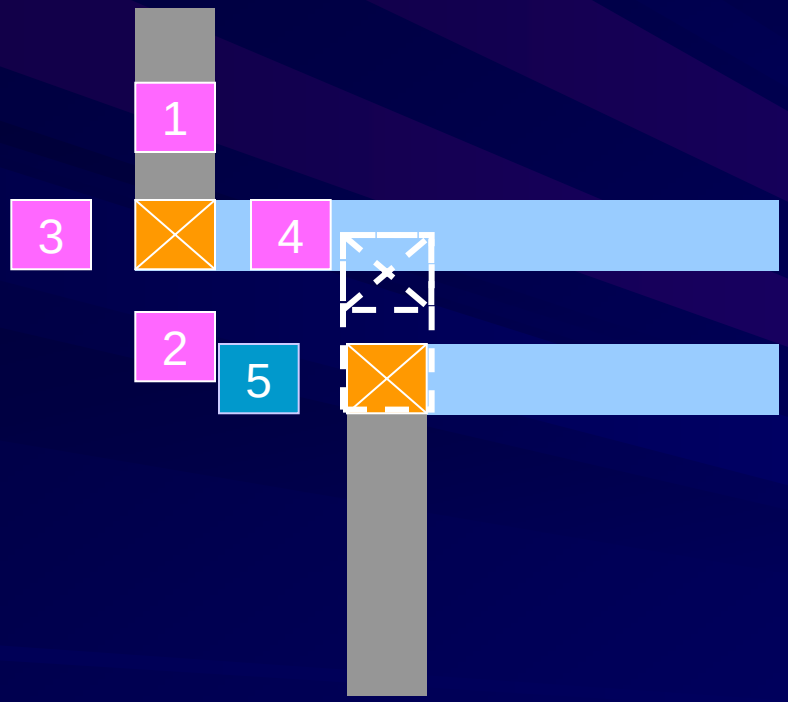
Graph construction

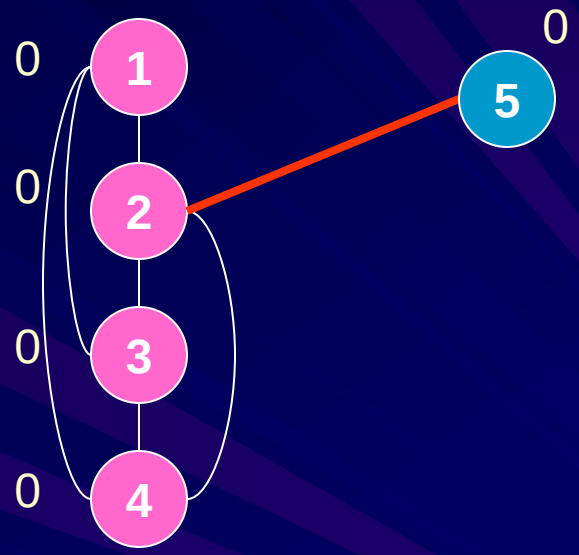
- **[Lee et al., ICCAD'06]**
  - **Sweep-line-like approach**
  - **Cannot consider wire bending**



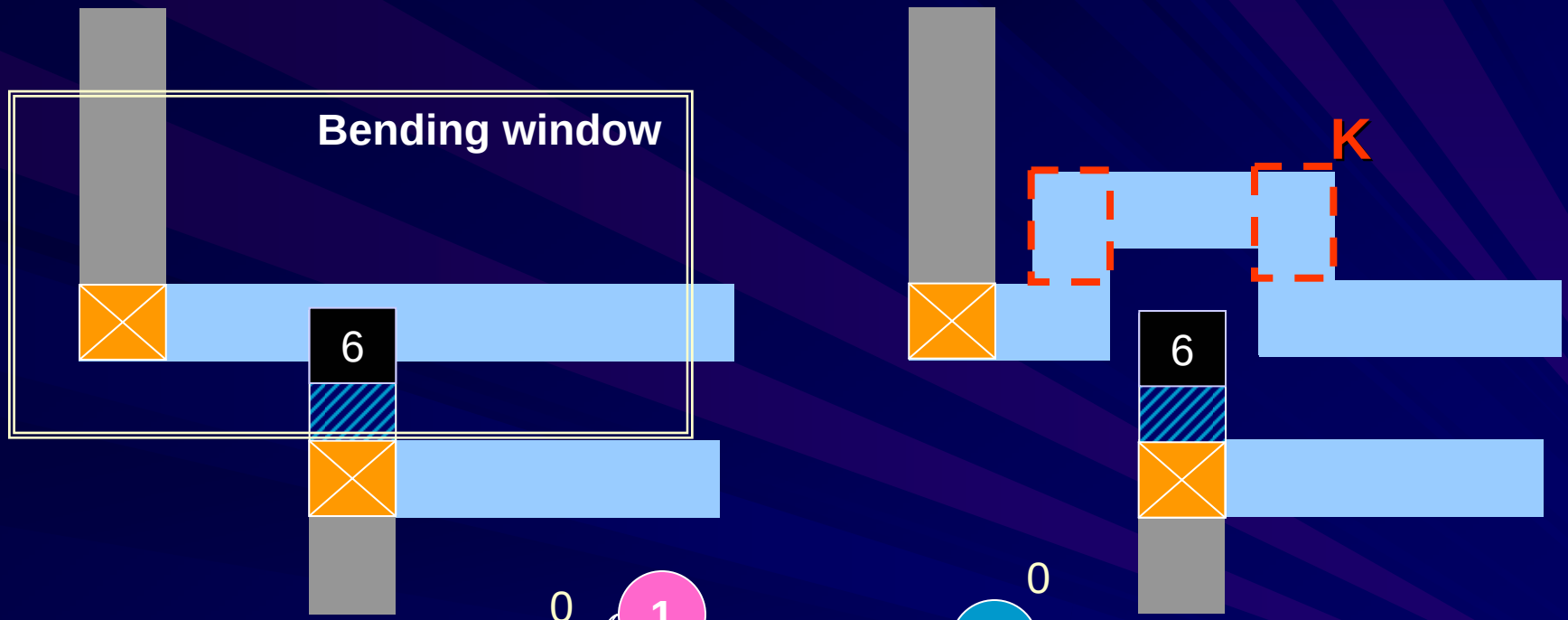


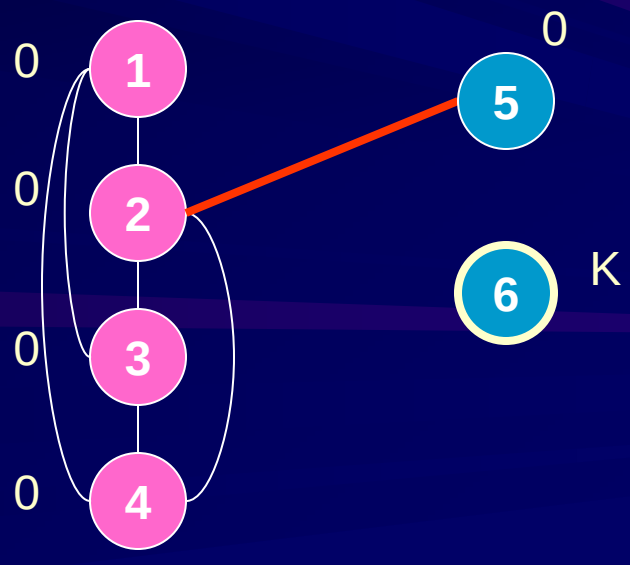
Graph construction



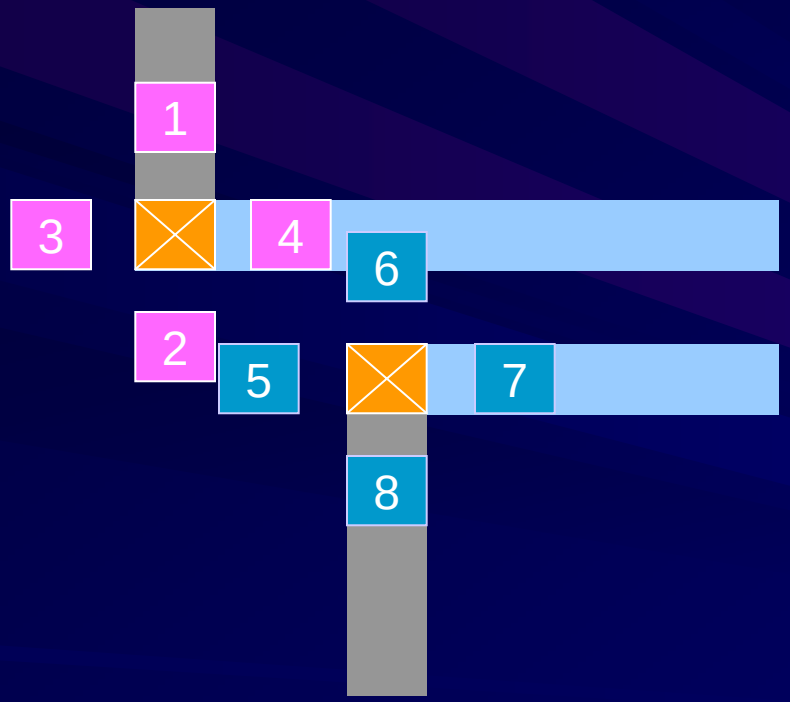


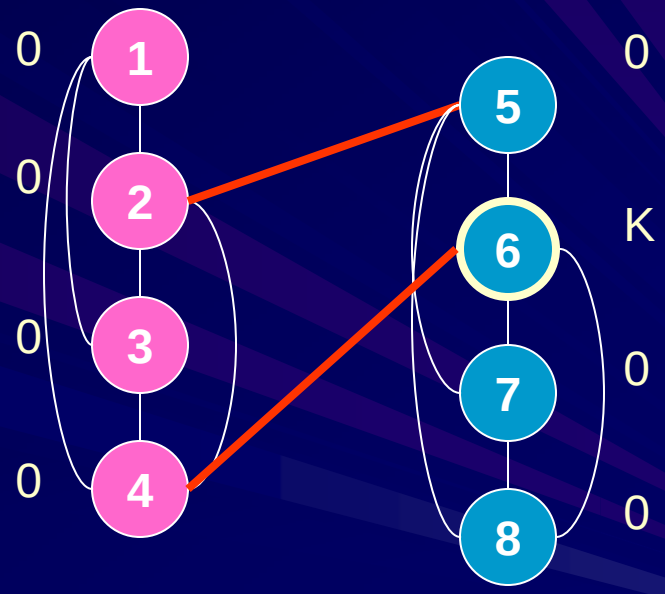
Graph construction





Graph construction





0-1 ILP formulation

of single vias

Weight of vertex *i*

Maximize $(C \cdot |SV|) \sum_{1 \le i \le 8} R_i - \sum_{1 \le i \le 8} W_i R_i$

$> \max W_i$

Subject to

$$R_1 + R_2 + R_3 + R_4 \le 1$$

$$R_5 + R_6 + R_7 + R_8 \le 1$$

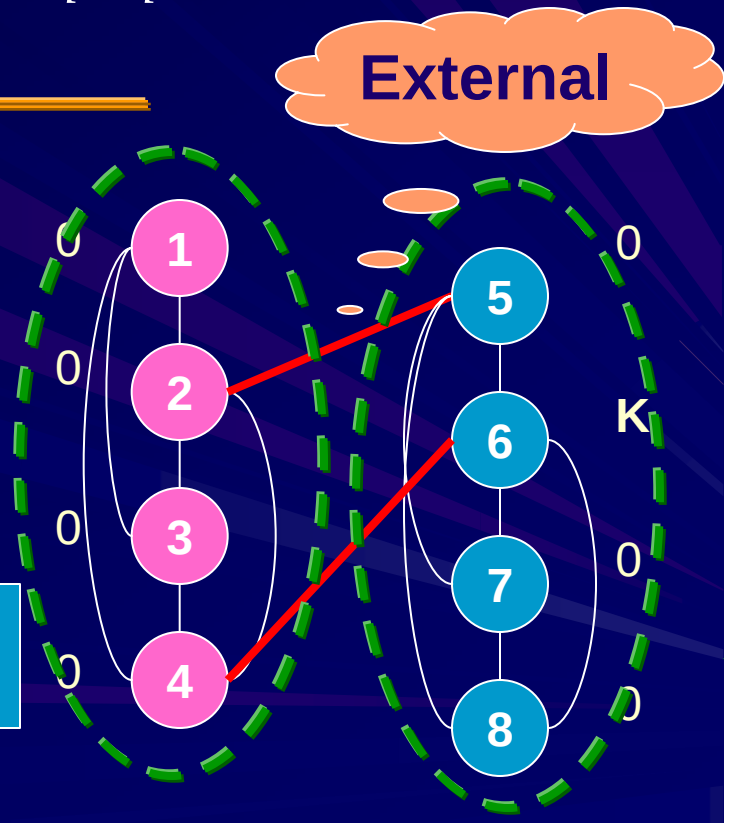
$$R_2 + R_5 \le 1$$

$$R_4 + R_6 \le 1$$

$$R_i \in \{0,1\}$$

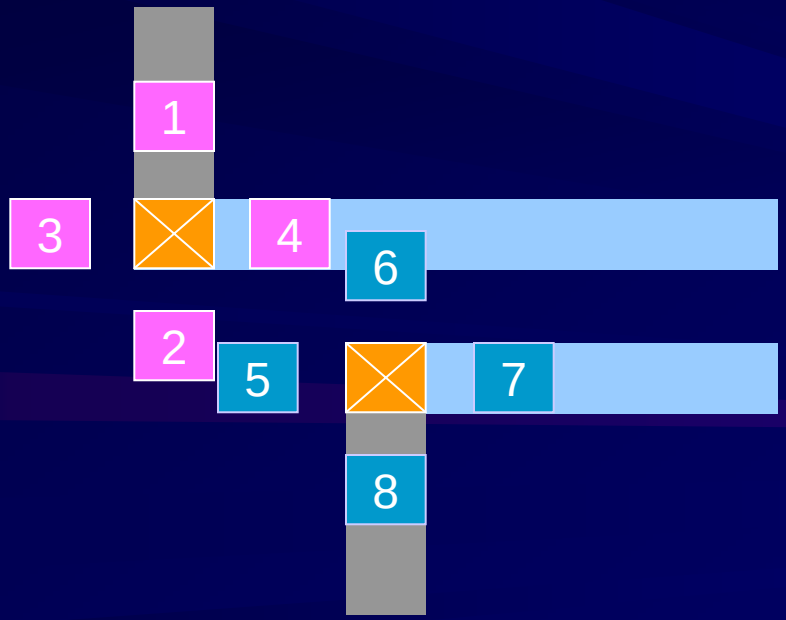
Double-cut constraint

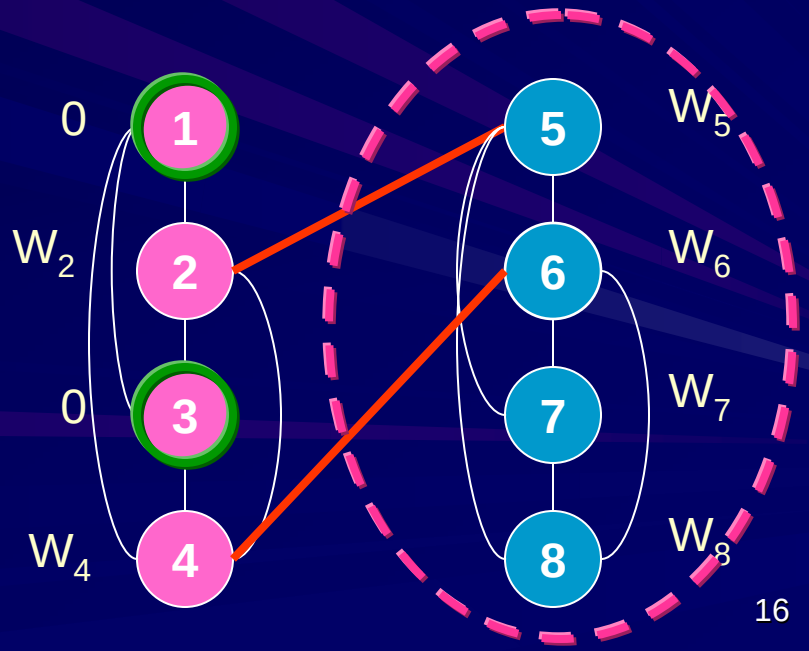
Conflict constraint



Speed-up – Pre-selection

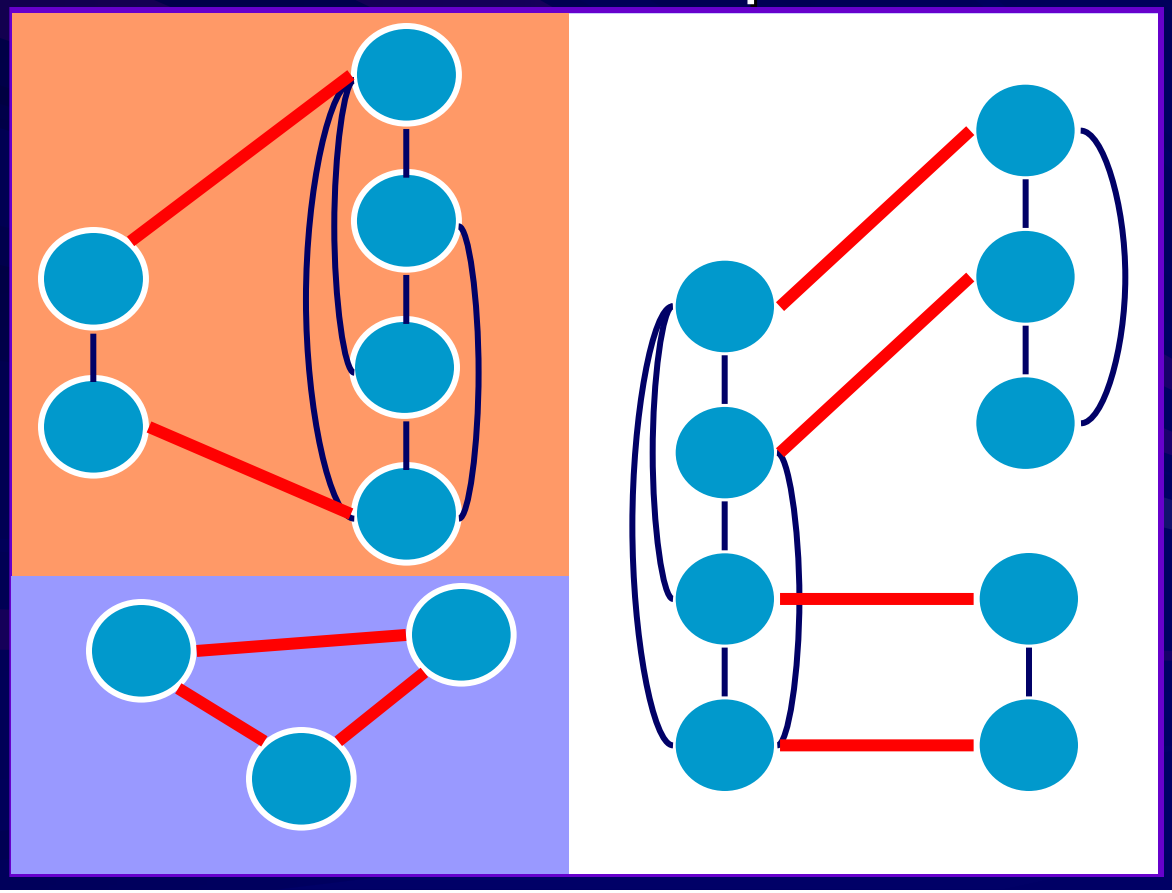
- Adapted from [Lee et al, ISPD'08]
  - No external edge
  - Having the minimum weight among the vertices coming from the same single via



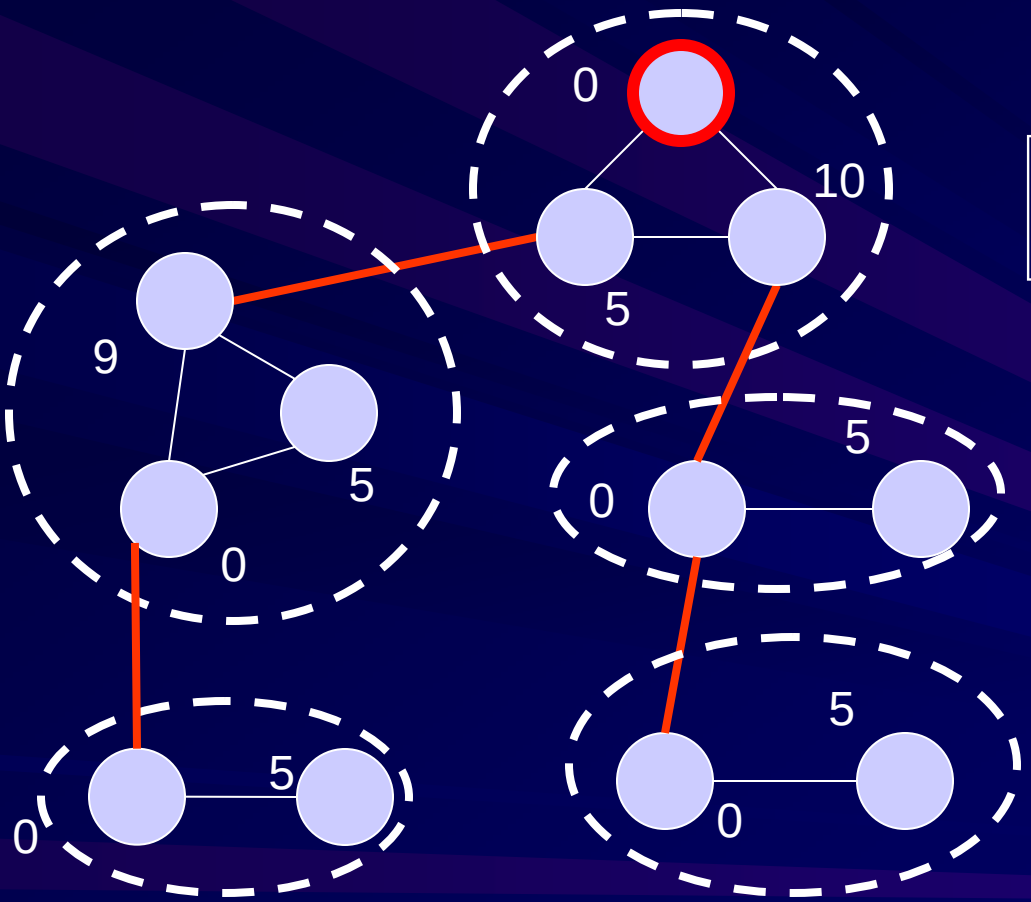


Speed-up – Connected components

- [Lee et al, ISPD'08]
  - Divide into smaller 0-1 ILP problems

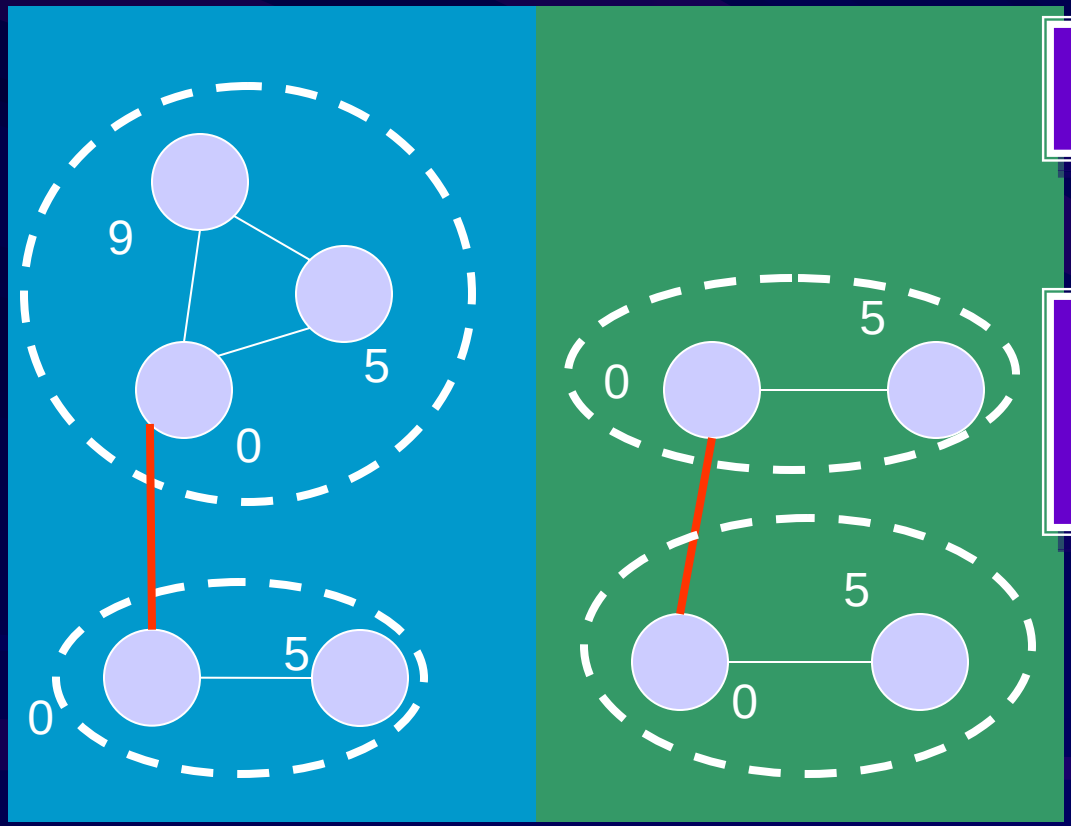


Overall approach



1. Pre-selection

Overall approach



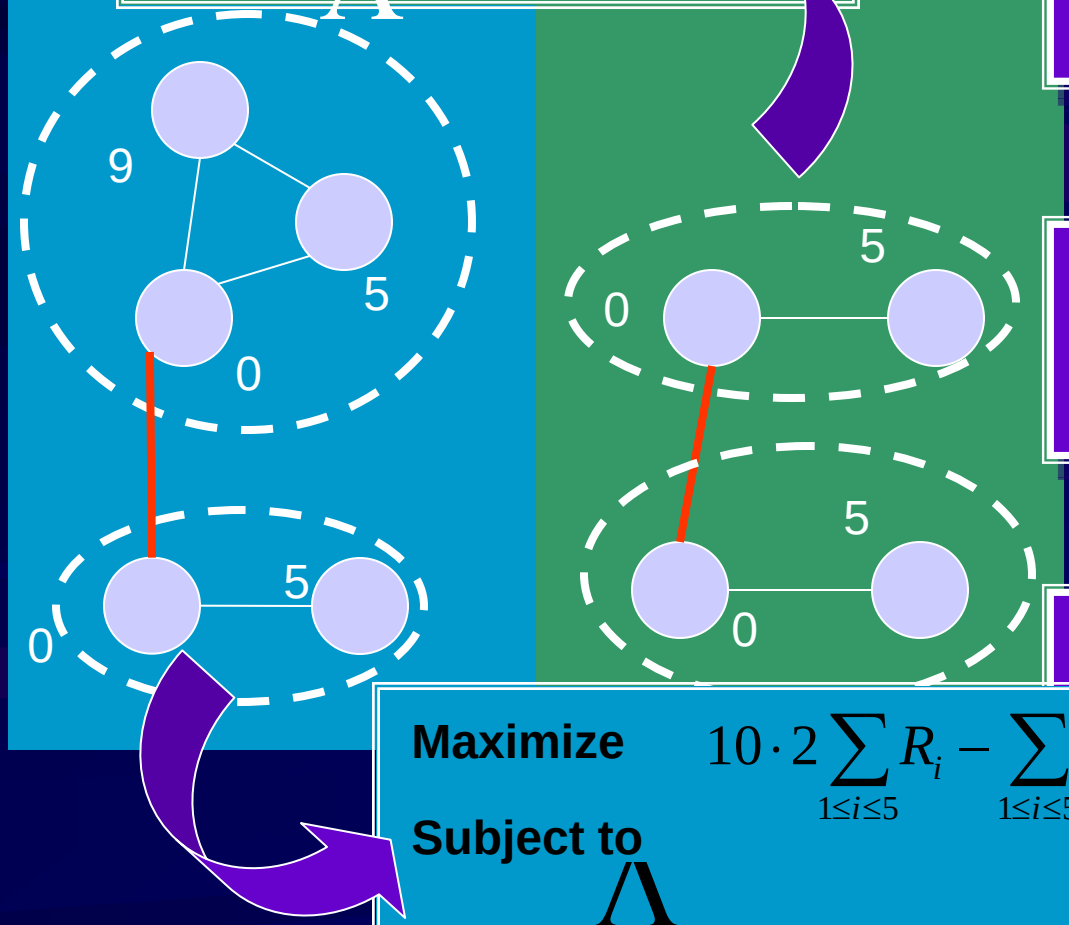
1. Pre-selection

2.Connected Components

Overall approach

Maximize $6 \cdot 2 \sum_{1 \le i \le 4} R_i - \sum_{1 \le i \le 4} W_i R_i$

Subject to Λ

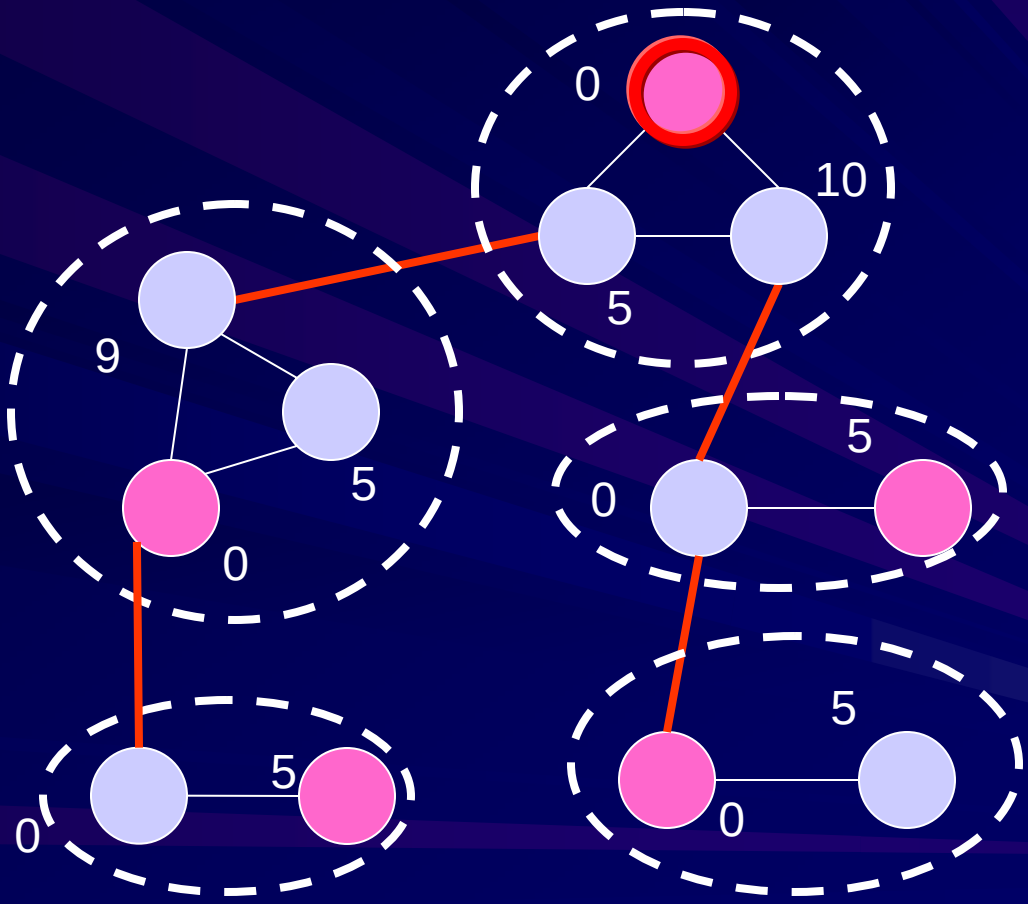


Maximize $10 \cdot 2 \sum_{1 \le i \le 5} R_i - \sum_{1 \le i \le 5} W_i R_i$

Subject to Λ

1. Pre-selection
2. Connected Components
3. Solve 0-1 ILP

Overall approach (cont'd)



Experiment setup

- Linux based machine with 2.4GHz processor and 2GB memory
- Adopted lp_solve as our 0-1 ILP solver

Circuit	#Nets	#I/Os	#Vias	#M-Layers
C1	4309	20	24594	5
C2	5252	211	41157	5
C3	18157	85	127059	5
C4	17692	415	151912	5
C5	44720	99	357386	5

Experimental results – Effectiveness of wire bending

Circuit	w/o wire bending				with wire bending			
	#A-vias	|V|	|E|	T(s)	#A-vias	|V|	|E|	T(s)
C1	19796	43246	36714	22	20664	53504	64083	27
C2	31464	67312	54376	32	33174	90541	114497	41
C3	99142	215647	179307	120	104356	284072	357643	157
C4	112076	220538	159691	131	119795	302904	371024	184
C5	276032	574142	444754	442	296323	804268	1025320	731
Normalized	1	1	1	1	1.06	1.33	2.09	1.36

Experimental results – # of inserted double vias

Circuit	01ILP–DVI*		01ILP–DVI/WB		
	#DVI	T(s)	#DVI	#WB	T(s)
C1	19754	3.23	20567	835	3.37
C2	31411	3.30	33101	1720	3.54
C3	98888	3.81	103934	5146	4.87
C4	111657	3.87	119256	7798	5.19
C5	275437	5.14	295383	20256	13.62
Normalized	1	1	1.06	-	1.18

*[Lee et al., ISPD'08]

Experimental results – Wirelength increase

Circuit	ECG + 01ILP–DVI*			01ILP–DVI/WB		
	WL(μ m)	Rate(%)	T(s)	WL(μ m)	Rate(%)	T(s)
C1	3.22E+03	0.32	3.30	9.96E+02	0.10	3.37
C2	8.21E+03	0.39	3.43	2.12E+03	0.10	3.54
C3	2.47E+04	0.39	4.42	6.30E+03	0.10	4.87
C4	3.11E+04	0.32	4.41	9.79E+03	0.10	5.19
C5	9.27E+04	0.36	9.02	2.57E+04	0.10	13.62
Normalized	1	-	1	0.28	-	1.22

*[Lee et al., ISPD'08]

Conclusions

- We studied the DVI/WB problem and formulated it as a mWMIS on the enhanced conflict graph
- We proposed an efficient 0-1 ILP based approach to solve the mWMIS problem
- The experimental results were shown to support our approach

Wire bending